SPECIFICATION

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METHODS AND APPARATUS FOR AMPLIFICATION IN HIGH TEMPERATURE ENVIRONMENTS

Federal Research Statement

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Background of Invention

[0001] This invention relates generally to methods and apparatus for amplification and signal processing at elevated temperatures, and more particularly to methods and apparatus for chopper stabilized amplification at high temperatures.

[0002] Amplification and signal processing of signals from sensors in high temperature environments are difficult tasks due to the failure of silicon devices to operate above 200 degrees Celsius. Amplifiers utilizing silicon carbide (SiC) semiconductors have been demonstrated, and SiC material itself is capable of operation at temperatures beyond 500 degrees Celsius. However, oxide interfaces in SiC metal on semiconductor (MOS) devices used in amplifiers contain many interface states, which introduce large random offsets that change as a function of temperature. The resulting amplifier offset drift makes it difficult to accurately amplify small sensor signals.

[0003] Techniques are known for offset drift reduction in amplifiers implemented with other semiconductor technologies. At least some known techniques include chopper stabilization, continuous offset removal using a second auxiliary *amplifier, and* correlated double sampling. However, these techniques have not been practical for amplifiers

utilizing SiC technology and other negative-channel metal-oxide semiconductor (NMOS) depletion mode technologies. Circuits in SiC technology with large numbers of transistors are subject to low yields due to micropipes and other material defects. Silicon carbide positive-channel MOS (PMOS) devices have low mobility, thus making it impossible to provide complementary circuits with switches. At present, depletion mode NMOS transistors are viable and reliable, but the negative thresholds of NMOS depletion mode transistors have complicated adaptation of conventional stabilization circuitry to SiC and other NMOS depletion mode processes.

Summary of Invention

[0004] There is therefore provided, in one aspect, a method for amplifying a signal including generating an input signal and amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal.

[0005] In another aspect, there is provided a buffered field effect transistor logic (BFL) level-shifting/inverter circuit having an input, an NMOS depletion mode inverter responsive to the inverter stage input to produce an inverted output, a buffered field effect transistor logic (BFL) stage that includes a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between the first channel and the second channel, a first output at an electrical node between the voltage drop circuit and the first channel, and a second output at an electrical node between the voltage drop circuit and the second channel.

[0006] In yet another aspect, there is provided an operational amplifier circuit including a first NMOS depletion mode amplification stage, a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to the first amplification stage, a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from the first amplification stage, and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate the first chopping signal and the level shifted first chopping signal across a voltage dropping element.

[0007] In still another aspect, there is provided an operational amplifier circuit including a first NMOS depletion mode amplification stage having differential inputs and outputs, a first NMOS depletion mode chopping switch responsive to a first chopping signal and a second chopping signal to chop a differential input signal to the first amplification stage, a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal and a level shifted second chopping signal to chop an output signal from the first amplification stage, a first NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate the first chopping signal and the level shifted first chopping signal across a first resistor, a second NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to the clock signal to generate the second chopping signal and the level shifted second chopping signal across a second resistor, and a clock generator circuit configured to generate the clock signal.

Brief Description of Drawings

[0008] Figure 1 is a simplified block diagram showing the topology of one embodiment of a depletion mode chopper-stabilized operational amplifier (op amp).

[0009] Figure 2 is a schematic diagram of one embodiment of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifter/inverter that suitable for use in the operational amplifier represented in Figure 1.

[0010] Figure 3 is a schematic diagram of a second embodiment of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifter/inverter that suitable for use in the operational amplifier represented in Figure 1.

[0011] Figure 4 is a schematic diagram of a portion of one embodiment of an NMOS depletion mode chopper-stabilized operational amplifier, excluding the clock generator shown in Figure 1 and the NMOS depletion mode BFL level/shifter inverters shown in Figures 1 and 2.

Detailed Description

[0012] As used herein, an element or step recited in the singular and preceded with the word "a" or "an" should be understood as not excluding plural said elements or steps, unless such exclusion is explicitly recited. Furthermore, references to "one embodiment" of the